High-Performance 40nm Gate Length InSb P-Channel Compressively Strained Quantum Well Field Effect Transistors for Low-Power (V_{CC}=0.5V) Logic Applications

M. Radosavljevic, T. Ashley*, A. Andreev*, S. D. Coomber*, G. Dewey, M. T. Emeny*, M. Fearn*, D. G. Hayes*, K. P. Hilton*, M. K. Hudait, R. Jefferies*, T. Martin*, R. Pillarisetty, W. Rachmady, T. Rakshit, S. J. Smith*, M. J. Uren*, D. J. Wallis*, P. J. Wilding* and Robert Chau
Intel Corporation, Technology and Manufacturing Group, Hillsboro, OR 97124, USA
*QinetiQ, Malvern Technology Centre, St Andrew's Road, Malvern, WR14 3PS, UK
Contact: robert.s.chau@intel.com

Abstract

This paper describes for the first time, a high-speed and low-power III-V p-channel QWFET using a compressively strained InSb QW structure. The InSb p-channel QW device structure, grown using solid source MBE, demonstrates a high hole mobility of 1,230cm^2/V-s. The shortest 40nm gate length (L_G) transistors achieve peak transconductance (G_m) of 510µS/µm and cut-off frequency (f_T) of 140GHz at supply voltage of 0.5V. These represent the highest G_m and f_T ever reported for III-V p-channel FETs. In addition, effective hole velocity of this device has been measured and compared to that of the standard strained Si p-channel MOSFET.

Introduction

The III-V compound semiconductor quantum-well field effect transistor (QWFET) is one of the most promising device candidates for future high-speed, low-power logic applications due to its high electron mobility. Recently, high-performance III-V n-channel QWFETs have been demonstrated [1-4]. However, for implementation of CMOS logic, there is a significant challenge of identifying high mobility III-V p-channel candidates [5]. In this work, we demonstrate for the first time a high-speed and low-power III-V p-channel QWFET using a compressively strained InSb QW structure, which achieves cut-off frequency (f_T) of 140GHz at transistor gate length (L_G) of 40nm and supply voltage (V_{CC}) of 0.5V. This represents the highest f_T ever reported for III-V p-channel FETs.

Materials Growth and Characterization

Fig. 1 shows the InSb p-channel QW device structure used in this work. The structure is grown on (100) GaAs substrates using solid source MBE. The biaxial compressive strain in the InSb QW is modulated between 1.0-2.0% using different Al composition in the $Al_xIn_{1-x}Sb$ barrier layers ($0.15 \leq x \leq 0.35$). Fig. 2 shows the band diagram of InSb p-channel compressively strained QWFET, indicating hole carrier confinement in the QW layer. Fig. 3 shows the high-resolution X-ray rocking curve from the (004) Bragg lines of InSb QWFET structure with different Al compositions in the barrier layers. The shift in angular position of the $Al_xIn_{1-x}Sb$ peak with respect to GaAs indicates increasing compressive strain in the InSb QW with increasing Al composition. Fig. 4 shows the 8-band k.p simulation of the in-plane effective hole mass as a function of energy for different compressive strain levels in the InSb QW. For a given energy, higher compressive strain results in lower in-plane effective hole mass. Fig. 5 shows the measured hole mobility vs. sheet carrier density for the InSb QW at room temperature indicating mobility improvement with increasing compressive strain and remote doping. The highest InSb QW hole mobility of 1,230cm^2/V-s is achieved with 1.9% compressive strain using $Al_{0.35}In_{0.65}Sb$ barrier layers along with remote doping. This hole mobility is >5X higher than that of standard strained Si p-channel MOSFET. Fig. 6 shows TEM image of the InSb p-channel 1.9% compressively strained QWFET structure grown on GaAs substrate, which suggests that misfit and threading dislocations are predominantly contained in the bottom barrier layers.

Device Fabrication and Characterization

The TEM image in Fig. 7 shows the 40nm gate length InSb p-channel QWFET with the $Al_{0.35}In_{0.65}Sb$/InSb QW/$Al_{0.4}In_{0.6}Sb$ stack. Note that the measured hole mobility characteristic of this stack is matched to that of the 1.9% compressively strained InSb QW with remote doping in Fig. 5. A wet etch is used for gate recess resulting in a 10nm gate-to-channel separation. Ti/Au metallization is used for both gate and source/drain electrodes. Fig. 8 shows SEM micrograph of the same device. Fig. 9 shows drain current (I_D) and gate leakage (I_G) versus gate voltage (V_G) of p-channel InSb QWFET with L_G=125nm. At V_{DS}= -0.5V, the device exhibits threshold voltage (V_T) = -0.01V, subthreshold slope (SS) =90mV/dec and drain induced barrier lowering (DIBL) =80mV/V. SS and DIBL as a function of L_G for InSb p-channel QWFETs are shown in Fig 10. Figs. 11 & 12 show the I_D-V_G and the I_D-V_{DS} characteristics respectively of InSb p-channel QWFET for L_G=40nm. Fig. 13 shows transconductance (G_m) characteristics at V_{DS}= -0.5V of InSb p-channel QWFET with L_G=40nm. The peak G_m is 510µS/µm, which is the highest ever reported for III-V p-channel FETs. Fig. 14 shows current gain (h_{21}) vs. frequency for the 40nm L_G InSb p-channel compressively strained QWFET, which achieves f_T=140GHz at V_{DS}= -0.5V. This represents the highest f_T ever reported for III-V p-channel FETs.

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Benchmarking vs. Standard Strained Si p-MOSFETs

Figs. 15 and 16 show gate delay (CV/I) vs. L_G and energy-delay product (CV^2*CV/I) vs. L_G, respectively, of InSb p-channel compressively strained QWFETs compared to Si p-channel MOSFETs. Other III-V p-channel QWFET work are included for reference [6, 7]. Compared to Si p-MOSFETs, the InSb p-channel QWFETs in this work show a reduction in gate delay and a significant improvement in energy-delay product, which represents the energy-efficiency of the device. Fig. 17 shows the cut-off frequency (f_T) as a function of DC power dissipation for InSb p-channel compressively strained QWFET with L_G=40nm at V_{DS}= -0.5V versus standard strained Si p-channel MOSFET transistor with L_G=60nm at V_{DS}= -0.5V and -1.1V. Compared to Si, InSb p-channel QWFET shows ~10X lower power at the same speed, or ~2X higher speed at matched power.

We have also extracted the effective hole velocity (v_{eff}) for both InSb p-channel QWFET and strained Si p-channel MOSFETs. This effective velocity is related to the transistor drive current in absence of parasitic resistance. v_{eff} is determined from the equation below [8, 9]:

$$\mathbf{v_{eff} = g_{mi}/(WC_{gi})}$$

where g_{mi} is the intrinsic saturated transconductance corrected for parasitic resistance, W is the width of the device, and C_{gi} is the intrinsic gate capacitance per unit area. In this work, both C_{gi} and g_{mi} of the InSb and Si devices are determined using high-frequency measurements and a small signal equivalent circuit model [9-11]. The high frequency response of the devices was measured from 1 to 50 GHz. Fig. 18 shows that the measured S parameters of the InSb p-channel QWFET are matched (with an RMS error of less than 1%) to its simulated S parameters based on the small signal equivalent circuit model. Fig. 19 shows the frequency independent signature of C_{GS}, which is the gate-source capacitance. Next, C_{gi} is determined from the slope of the total gate capacitance (C_{GS} + C_{GD})/W versus the various physical gate lengths of the devices where C_{GD} is the gate-drain capacitance. The RMS error of less than 1 % between measured and modeled S parameters and the frequency independent signature of small signal circuit elements allow for accurate extraction of g_{mi}, C_{gi}, and thus the effective hole velocity of both InSb and Si. Fig. 20 shows the effective hole velocity (v_{eff}) vs. DIBL comparing InSb p-channel QWFETs to strained Si p-channel MOSFETs at V_{DS}= -0.5V and $|V_G-V_T|$=0.3V. It is observed that v_{eff} in InSb p-channel QWFETs is >2X higher than that of strained Si p-channel MOSFETs for the same DIBL, demonstrating the intrinsic advantages of InSb p-channel QWFETs over Si p-channel MOSFETs. Further improvement in v_{eff} of the p-channel InSb QWFET for a given DIBL will require further optimization of the device such as reduction of the gate-to-channel separation and increase in strain.

Conclusions

High performance 40nm gate length InSb p-channel compressively strained QWFETs have been fabricated and achieved f_T=140GHz at V_{DS}= -0.5V. Compared to standard strained Si p-MOSFET, the InSb p-channel QWFET exhibits ~10X lower power dissipation for same speed, or ~2X improvement in speed for same power dissipation. Furthermore, v_{eff} in InSb p-channel QWFETs shows more than 2X improvement compared to strained Si p-channel MOSFETs for the same DIBL, demonstrating intrinsic advantages of InSb QWFETs as a PMOS option for the III-V CMOS configuration.

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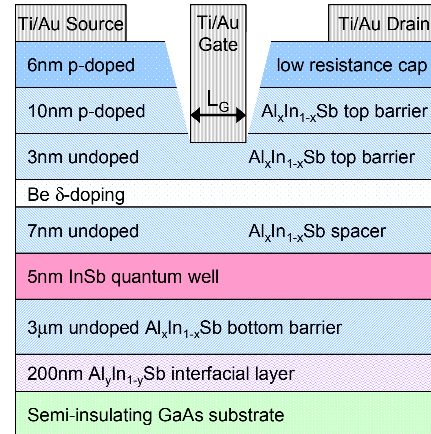

Fig. 1: Schematic of InSb p-channel compressively strained QWFET structure on GaAs. Al composition (x) in the barrier layers is varied from 0.15 to 0.35 to provide compressive strain and hole confinement in the InSb QW.

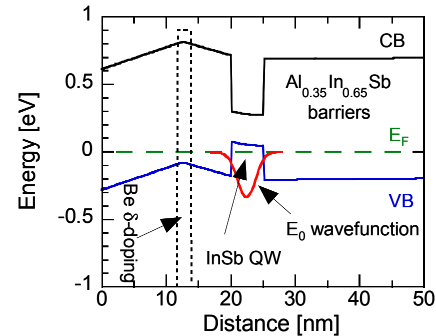

Fig. 2: Band diagram of InSb p-channel 1.9% compressively strained QWFET obtained using 8-band **k.p** simulation, indicating hole carrier confinement in the QW layer. Valence band (VB), Fermi level (E_F) and conduction band (CB) are shown.

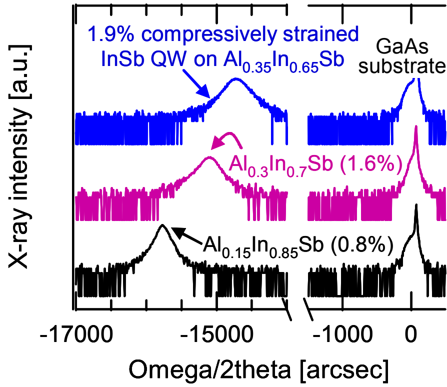

Fig. 3: High-resolution X-ray rocking curve from the (004) Bragg lines of InSb p-channel compressively strained QWFET structure with different Al compositions. The shift in angular position of the $Al_xIn_{1-x}Sb$ peak with respect to GaAs indicates increasing compressive strain in the InSb QW with increasing Al composition.

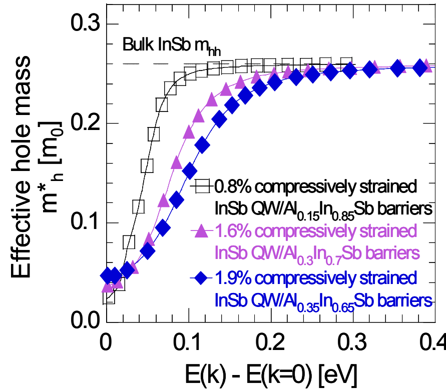

Fig. 4: 8-band **k.p** simulation of in-plane effective hole mass as a function of energy for different compressive strain levels in InSb QW. For a given energy, higher compressive strain results in lower effective hole mass.

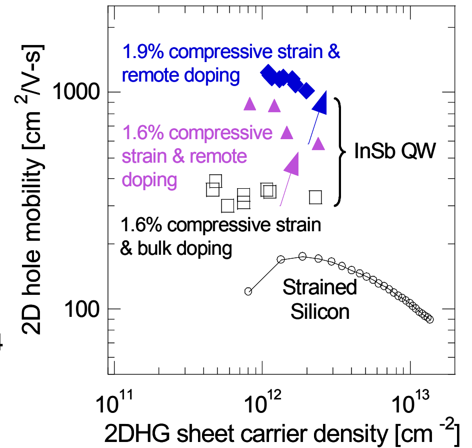

Fig. 5: Hole mobility vs. sheet carrier density measurements for InSb QW showing mobility improvement with increasing compressive strain and remote doping. The best hole mobility in InSb QW is 5X higher than that of standard strained Si p-channel MOSFET.

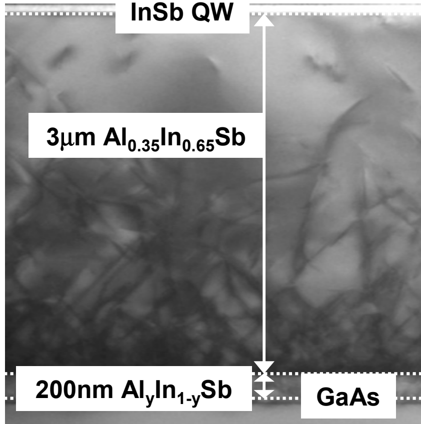

Fig. 6: Cross-sectional TEM image of InSb p-channel compressively strained QWFET structure grown on the (100) GaAs substrate. The misfit and threading dislocations are predominantly contained in the buffer layer.

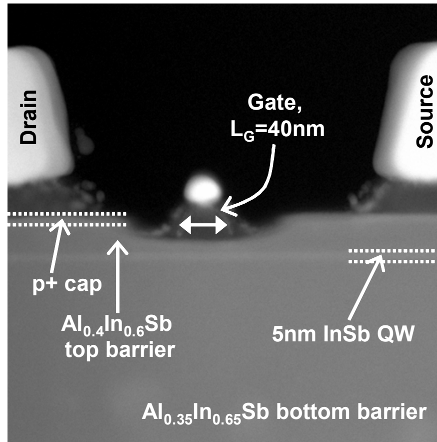

Fig. 7: High-magnification TEM image of the 40nm gate length InSb p-channel compressively strained QWFET, showing the $Al_{0.35}In_{0.65}Sb$ bottom barrier, InSb QW and $Al_{0.4}In_{0.6}Sb$ top barrier.

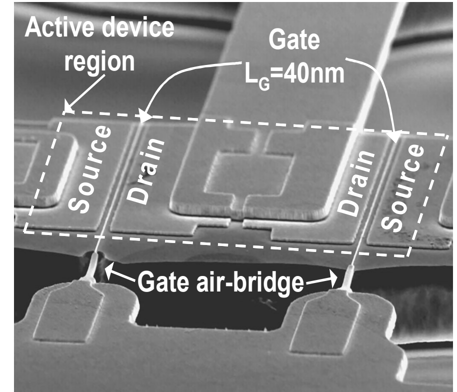

Fig. 8: SEM micrograph of a 40nm gate length InSb p-channel compressively strained QWFET with gate air-bridge suitable for RF characterization.

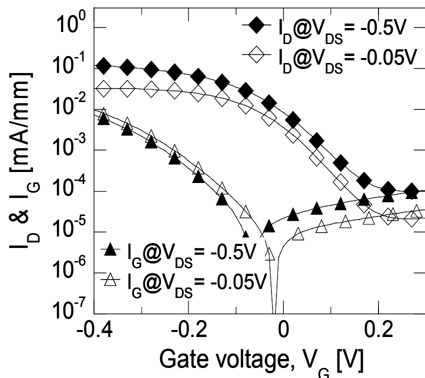

Fig. 9: Drain current (I_D) and gate leakage (I_G) versus gate voltage (V_G) of InSb p-channel compressively strained QWFET with L_G=125nm. At V_{DS}=-0.5V the device shows threshold voltage (V_T) = -0.01V, subthreshold slope (SS) =90mV/dec and drain induced barrier lowering (DIBL) =80mV/V.

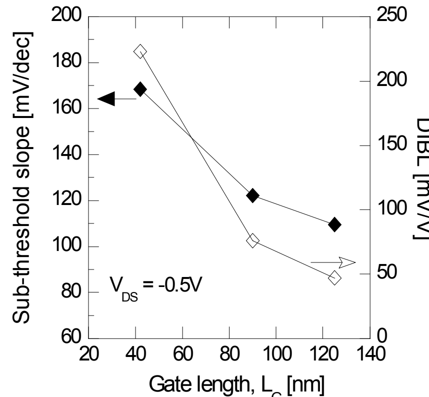

Fig. 10: Sub-threshold slope and DIBL as a function of L_G for InSb p-channel compressively strained QWFETs.

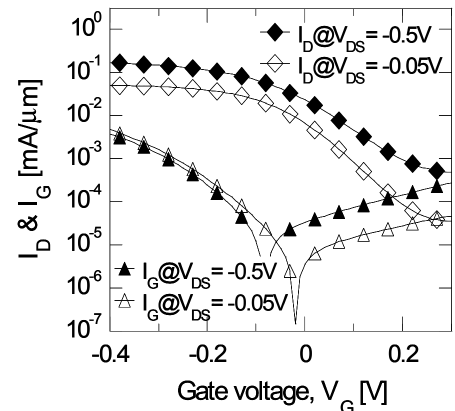

Fig. 11: I_D and I_G vs. V_G of InSb p-channel compressively strained QWFET with L_G=40nm. At V_{DS}= -0.5V the device shows V_T= +0.03V, SS=160mV/dec and DIBL=220mV/V.

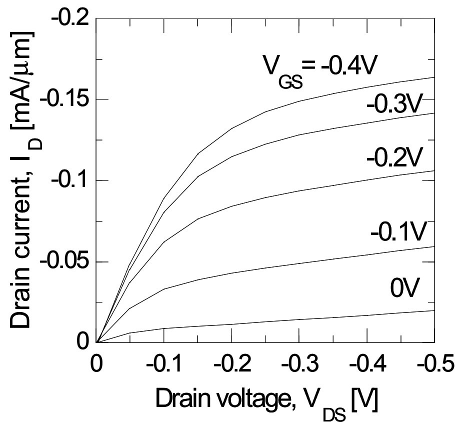

Fig. 12: I_D-V_{DS} characteristics of InSb p-channel compressively strained QWFET with L_G=40nm.

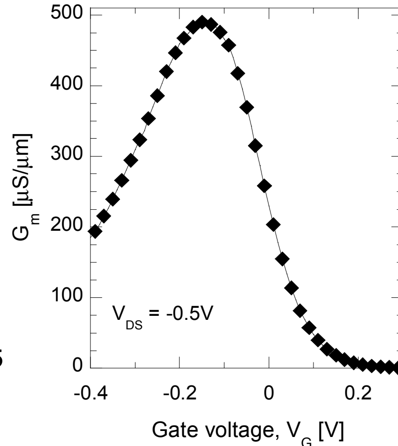

Fig. 13: Transconductance (G_m) characteristics of InSb p-channel compressively strained QWFET with L_G=40nm. Peak G_m is 510µS/µm at V_{DS}= -0.5V, which is highest ever reported for III-V p-channel FET.

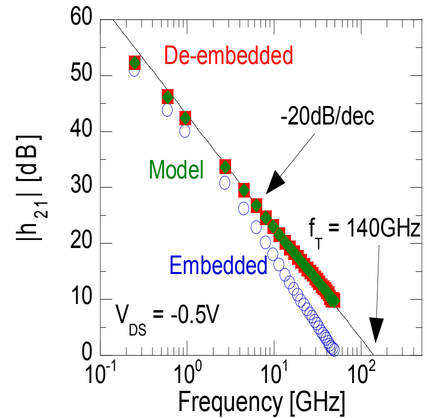

Fig. 14: Current gain (h_{21}) vs. frequency for the 40nm L_G InSb p-channel compressively strained QWFET, showing embedded and de-embedded RF data. The InSb p-channel device achieves f_T =140GHz at V_{DS}= -0.5V.

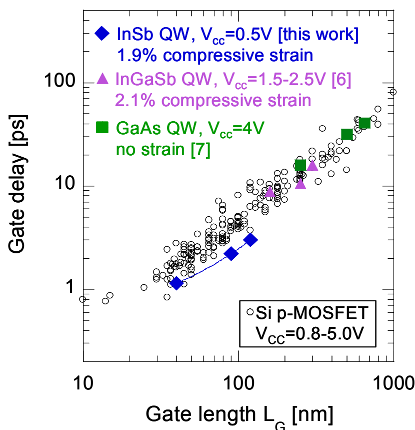

Fig. 15: Gate delay (CV/I) vs. L_G of InSb p-channel compressively strained QWFETs compared to production and research Si p-MOSFET data. Other III-V p-channel QWFET work are included for reference [6, 7].

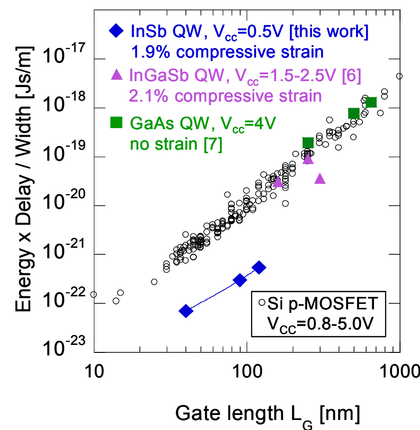

Fig. 16: Energy-delay product vs. L_G comparing InSb p-channel compressively strained QWFETs with production and research Si p-MOSFET data. Other III-V p-channel QWFET work are included for reference [6, 7].

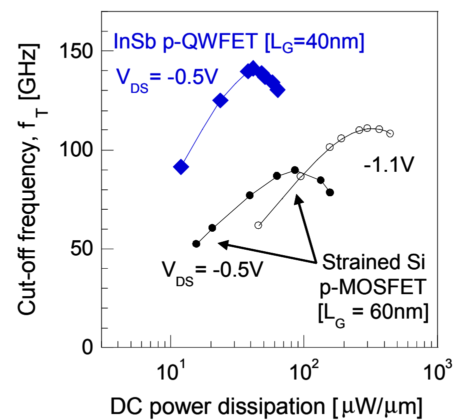

Fig. 17: Cut-off frequency as a function of DC power dissipation for InSb p-channel compressively strained QWFET with L_G=40nm at V_{DS}= -0.5V vs. standard strained Si p-channel MOSFET transistor with L_G=60nm at V_{DS}= -0.5V and -1.1V.

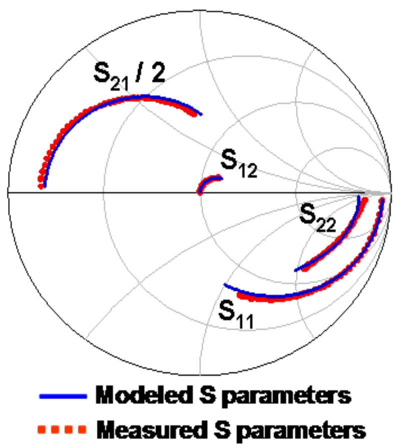

Fig. 18: Simulated S parameters based on a small signal equivalent circuit model and measured S parameters of the p-channel InSb QWFET from 1 to 50 GHz. The RMS error between measured and modeled S parameters is less than 1%.

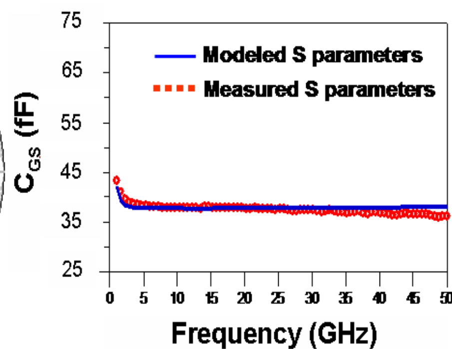

Fig. 19: Comparison between gate-to-source capacitance (C_{GS}) simulated by the circuit model and extracted from the measured S-parameters of the p-channel InSb QWFET. The frequency independent nature of capacitance and other circuit elements allows accurate extraction of v_{eff}.

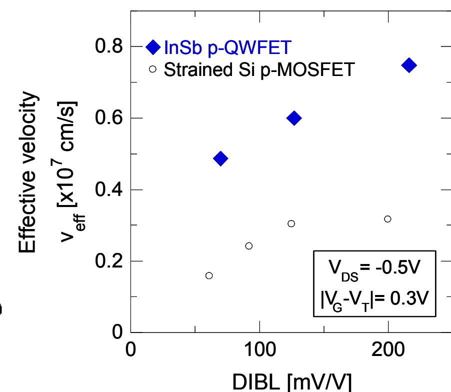

Fig. 20: Effective hole velocity (v_{eff}) vs. DIBL comparing InSb p-channel compressively strained QWFETs to strained Si p-channel MOSFETs at V_{DS}= -0.5V and $|V_G$-$V_T|$=0.3V. InSb p-channel QWFETs show more than 2X gain in v_{eff} over Si at matched DIBL.